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PATENT APPLICATION
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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ADRIENNE CHOCHOLAK
(SENDER'S PRINTED NAME) (SIGNATURE)

Box Patent Application
Assistant Commissioner for Patents
Washington, D.C. 20231

Enclosed for filing is a patent application under 37 CFR 1.53(b) of:

Inventor Sang-Eun LEE and Jae-Sung HAN:
For: METHOD OF IDENTIFYING AND ANALYZING SEMICONDUCTOR CHIP DEFECTS

Applicant requests FIG. 1 to be published with the application.

Enclosures:
☒ Specification (pages 1-7); claims (pages 8-10); abstract (page 11)
☒ SEVEN sheet(s) of FORMAL drawings
☒ Declaration or Combined Declaration and Power of Attorney
☒ Newly executed (original or copy)
☒ Assignment with cover sheet
Assignee Name and Address: Samsung Electronics Co., Ltd.
Suwon-city, Kyungki-do, Korea
☒ Certified copy of Priority Document No. 2001-8465, filed February 20, 2001
☒ Return Postcard

CLAIMS AS FILED				
For	Number Filed	Number Extra	Rate	Basic Fee $740
Total Claims	20-20	0	x $ 18 =	0
Independent Claims	3-3	0	x $ 84 =	0
TOTAL FILING FEE				$740

☒ PTO Form 2038 authorizing credit card payment for the above-listed fees is enclosed.
☒ Any deficiency or overpayment should be charged or credited to deposit account number 13-1703. A duplicate copy of this sheet is enclosed.

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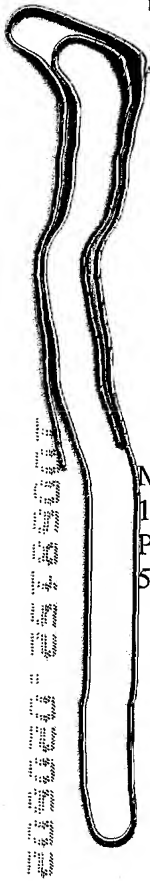

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METHOD OF IDENTIFYING AND ANALYZING SEMICONDUCTOR CHIP DEFECTS

Cross Reference

This application claims priority, under 35 U.S.C. § 119, from Korean Patent Application No. 2001-8465, filed on February 20, 2001, the contents of which are incorporated herein by reference in their entirety.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to methods of identifying semiconductor chip defects on a wafer and classifying those defects based on the type of defect. More particularly, this invention relates to using semiconductor inspection instruments to identify, analyze, and display the number and type of chip defects generated in a wafer.

2. Description of the Related Art

In the field of Defect Review Tools (DRTs), several instruments are widely used to identify and analyze chip defects. For example, Scanning Electron Microscopes (SEMs), made by Hitachi or KLA, and a Focused Ion Beam (FIB), made by FEB, are all widely used for this purpose. In addition to the foregoing instruments, which are used to image defect sources for review, the recent technological trend has been toward developing an instrument for identifying the cause of these defects by determining the composition of the defect. Commercial instruments implementing this trend have been introduced in the market. The goal of this trend is to overcome technological limits expected to be encountered in defect reduction in around the year 2003. This trend is expected to accelerate during upcoming decades.

Unfortunately, even though these newly introduced DRT instruments that analyze defects based on composition have already helped obtain cleanness levels of Class 1, problems have been encountered in identifying chip defect causes based on defect composition. In particular, defect data obtained using these instruments is complicated. Anyone other than a highly trained specialist therefore has difficulty understanding the defect data obtained by the DRT instrument. A mass production implementation of these DRT instruments is therefore impractical without better analysis tools.

Defect management in mass production of semiconductor products is critical because defects are directly related to mass production yields. Presently, defects are classified according to size using instruments such as SEMs or an AIT, and are classified according to type using instruments having a review station, such as an INS3000 made by Leica.

Defect classifications using these tools, however, remain in a primitive state and can include numerous operator errors. These errors impede the recent trend toward miniaturization of semiconductor devices. Additional analysis is therefore required before defects can be eliminated. In addition, even though some analysis is typically performed to help eliminate defects, it is difficult to correctly classify and analyze defects according to type using the prior art classification methods.

Furthermore, despite the amount of information obtained, that information alone is not sufficient to determine the cause of individual defects. In other words, even though statistical classification and management of the defects is possible, using the information obtained, the information regarding individual defects is not sufficient to determine the cause of that defect. Additional analysis is therefore necessary to get the desired information relating to individual defects.

FIG. 4a is a wafer defect map according to the prior art. The wafer defect map of FIG. 4 was obtained using the KLA SEM. FIG. 4b is a bar graph of defects classified by type according to the prior art. The data in FIG. 4b was analyzed in a conventional instrument having a review station using the defect map of FIG. 4a.

In the conventional defect review process, pictures of the defects are generally taken using an optic or scanning electron microscope. Classification of defects by type is accomplished using the microscope pictures. When the defect problem in the wafer production process is serious, the cause of defects may also be analyzed by determining defect composition. However, the data obtained from the conventional component analysis is difficult to understand and requires careful review by a skilled technician.

The defects generated on a chip have a significant influence on the yield loss and on the inferiority of chip characteristics. It should be noted, however, that even when there are a hundred chips containing defects, the yield loss is generated in only between about 1 to 30 of those chips (i.e., about 1-30% of the chips having defects). The yield loss is not generated in the other 70 to 99 chips. In other words, the yield loss of one semiconductor process can be different from the yield loss of another process, even though the same number of chips with defects are generated in those processes. The yield loss may also differ according to the type of semiconductor device, as well as the size, location, and type of defect.

For example, a DRAM device chip cannot be produced when a defect exists in an area surrounding a memory cell. When the defect exists within the memory cell, however, the chip can still be used to produce a good chip. This is because a laser repairing process can be used to repair the chip using redundancy cells in the same chip. Accordingly, in DRAM devices, the yield loss depends more upon the position of the defects than on the number of defects.

Chip defects are not the only cause of yield loss in a semiconductor product. Defects in manufacturing processes, such as a photolithography process, an etching process, a diffusion process, an ion implanting process, and a thin film deposition process, can also result in chip failure. It is therefore often difficult to clearly identify the influence of chip defects on yield loss.

As described above, the degree of yield loss resulting from chip defects varies depending on the type of device being manufactured and the processes used to produce that device. In addition, the conditions in a semiconductor manufacturing plant, such as the equipment, surroundings, and treatments can also cause defects. Managing yield by managing defects is therefore extremely difficult.

Presently, the technology that uses chip defects to measure yield loss and identify inferior chip characteristics can identify a total number of defects on a wafer, a total number of defect chips, and can classify defects according to defect size and type. After matching these measurements with yield results, this data is analyzed in several ways. For example, a total number of chip defects is compared to the degree of yield loss as well as to the number of particular kinds of chip defects. The total number of chips having defects is also compared to the degree of yield loss and the number of particular kinds of defects in the chips.

Accordingly, only relative measurements of the yield loss are determined. The yield loss and the particular defect ratios are increased when the total number of defects and the total number of defect chips are increased. Because subsequent semiconductor processes can vary the yield loss in the produced semiconductor device, it is difficult to precisely determine at this stage how the defects will influence the ultimate yield loss. It is therefore also impractical to measure absolute values of the yield loss by the defects.

Korean Patent Application No. 1998-29089 discloses methods of measuring the number of chips in the yield loss and the number of defective chips, by type, based on the semiconductor chip defects. The method described in that application, however, can only properly manage and correctly measure the number of chips with defects in a unit process or

between unit processes. Information for each of the defects is insufficient to enable the desired analysis and a quick response to the chip defects is therefore difficult.

SUMMARY OF THE INVENTION

To overcome the foregoing problems, various preferred embodiments of the present invention provide an improved map of wafer defects, defect cause distribution charts, and a method of analyzing the causes of defects simply and quickly.

In a preferred embodiment of the present invention, a method of identifying and marking chip defects based on the cause of the defect is provided. Defects are first identified using a semiconductor defect inspection instrument. The defect inspection instrument is then used to analyze the composition of the defect to determine a cause thereof. The defects are thereafter marked on a wafer map using the same marks to represent defects caused in the same manner. Using these specially-coded markings, graphs and other charts can then be prepared to display distributions, skews, and other arrangements of defect characteristics. The defects can then be more readily analyzed statistically.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete understanding of the advantages of the present invention will be available through the following detailed description of preferred embodiments, made with reference to the following drawings, in which:

FIG. 1 is a wafer map identifying defect locations on a wafer by type, according to one aspect of the present invention;

FIG. 2 is a bar graph classifying defects based on causes thereof, according to another aspect of the present invention;

FIGS. 3A, 3B, and 3C are printouts of SEM, EDS, and AES results, respectively, for finding defects, identifying the type of defect, and analyzing the composition thereof, according to still another aspect of the present invention;

FIG. 4a is a wafer defect map according to the prior art; and

FIG. 4b is a bar graph representing the number of defects by defect type, according to the prior art.

DETAILED DESCRIPTION OF PREFFERED EMBODIMENTS

Various preferred embodiments of the present invention will now be described in further detail. Referring to FIG. 1, a wafer defect map 10a, according to one aspect of the

present invention, identifies the location of defects on the wafer using markings 100. In the wafer defect map of FIG. 1, like markings are used to represent defects of the same type. FIG. 2 is a bar graph illustrating a process of classifying the defects according to another aspect of the present invention.

Referring to FIGS. 1 and 2, a method of identifying and analyzing defects in semiconductor chips, according to a preferred aspect of this invention, will be described. One or more semiconductor defect inspection instruments are first used to identify the location and type of defects on a wafer. A Defect Review Tool (DRT), such as the KLA SEM, can be used for this purpose. After the defects have been located, the same defect inspection instrument, or a different inspection instrument, is used to determine the composition of the defects.

Referring to FIGS. 3A through 3C, the defect analysis is preferably performed by first taking a picture of the defect structure using a SEM. A sample SEM picture is shown in FIG. 3A. An EDS analysis can also be conducted on the defect, sample results of which are illustrated in FIG. 3B. An AES analysis can then be used to determine a composition of the defect. The results of the AES analysis on the defect of FIG. 3A are shown in FIG. 3C. A table is then preferably created and identifies the defects by number, and further specifies the type of defects, the process that resulted in the defect, the defect composition, and the position of the defects on the wafer. Table 1, for example, is constructed according to this aspect of the present invention.

Table 1

Defect No.	Classification of defect type using SEM equipment	Classification of process resulting in defect using the semiconductor inspection equipment	Classification of defect composition using AES equipment	Position of defect on a wafer
12	155	Al defect after TiN deposition	Al metal	Surface
13	155	Al defect after TiN deposition	Al Oxide, F	Surface
15	99	None		Pit
18	99	None		Pit
19	99	None		Pit
21	99	None		Pit
28	155	Si defect before TiN deposition		Buried area
29	155	Si defect before TiN		Buried area

		deposition		
30	155	Si defect before TiN deposition		Buried area
34	155	Si defect before TiN deposition	Si Metal	Buried area
38	155	Si defect before TiN deposition	Al Oxide	Buried area
39	155	Si defect before TiN deposition	Al Oxide	Surface
42	155	Si defect before TiN deposition	Al Oxide	Surface
45	155	Si defect before TiN deposition	Al Oxide	Surface

Referring back to FIG. 1, after the defect analysis is completed, a wafer map 10a is constructed using markings 100 to show the locations of the defects. The markings 100 are preferably used to identify both defect location and type, with like markings representing the same type of defect. The markings, for instance, can be dot marks, with dot colors assigned depending on defect type or the markings can have different shapes depending on defect type.

After the defects have been marked on the wafer map 10a, an inspection instrument, such as a review station, is used to categorize the defects based on various defect characteristics. The number and type of defects can be represented in a bar graph, such as that shown in FIG. 2 for instance, to facilitate a quick statistical analysis thereof. Bar graphs could also be created concurrently with the marking of defects on the wafer map 10a.

The defects can also be coded and analyzed electronically. In the electronic process, a defect inspection instrument is again preferably used to find the defects. Data corresponding to the defects is then coded and stored in files or in a database. The defect data can then be analyzed using an appropriate software program. Using this method, after existing defects have been identified and tabulated, defects generated in subsequent processes can be easily identified and analyzed in a short period of time.

According to these aspects of the present invention, wafer defects can be identified and statistically analyzed according to information obtained using defect recognition tools. This method can be used to quickly and efficiently identify the generation of defects during the mass production of semiconductor chips, so that the causes of those defects can be identified and prevented, resulting in an improved yield. Although the present invention has been shown and described with reference to preferred embodiments thereof, it will be

understood by those skilled in the art that various changes can be made in the form and details thereof without departing from the spirit and scope of the following claims.

CLAIMS

What is claimed is:

1. A method of classifying defect chips, said method comprising:

finding defect locations on a wafer using a semiconductor defect inspection instrument;

analyzing the defect composition using the semiconductor defect inspection instrument; and

marking defect locations on a wafer map using the same type of mark to identify of the same type of defect or defects containing similar compositions.

2. The method according to claim 1, wherein the marks on the wafer map are dot marks.

3. The method according to claim 2, wherein the dot marks are color coded according to defect type and/or defect composition.

4. The method according to claim 1, further comprising graphing defect characteristics concurrently with marking defect locations on the wafer map.

5. The method according to claim 1, further comprising storing and analyzing defect characteristics electronically using software.

6. The method according to claim 1, further comprising:

using the marks on the wafer map to prepare graphs to assist in statistically analyzing the defects.

7. A wafer defect map, comprising:

a schematic representation of a semiconductor wafer, including demarcations corresponding to the location of chip boundaries; and

a plurality of markings, each marking corresponding to a wafer defect,

wherein locations of the markings on the wafer map correspond to locations of the defects on the wafer, and wherein each marking is configured to identify a type of defect.

8. The wafer defect map according to claim 7, wherein the markings are color-coded to represent defect type.

9. The wafer defect map according to claim 7, wherein the markings have different shapes depending on defect type.

10. The wafer defect map according to claim 7, wherein the location and type of wafer defects is determined using a semiconductor defect inspection instrument.

11. A method of statistically analyzing defects on a semiconductor wafer to improve yield, said method comprising:

identifying a location and type of wafer defects;

determining a composition of the wafer defects;

preparing a wafer defect map to visually represent the location and type of the wafer defects; and

preparing one or more charts and/or graphs to statistically represent defect characteristics.

12. The method according to claim 11, wherein markings are placed on the wafer defect map corresponding to defect locations.

13. The method according to claim 12, wherein the markings are color-coded based on the type of defect represented thereby.

14. The method according to claim 11, wherein identifying a location and type of wafer defects comprises using an optical or scanning electron microscope to identify the location and type of wafer defects.

15. The method according to claim 11, wherein determining a composition of the wafer defects comprises performing an AES analysis on the defects to determine the compositions thereof.

16. The method according to claim 11, wherein preparing one or more charts and/or graphs comprises constructing a table comprising columns corresponding to defect type, defect composition, defect cause, and defect location.

17. The method according to claim 11, wherein preparing one or more charts and/or graphs comprises preparing a bar graphs representing the number of defects according to defect type.

18. The method according to claim 11, wherein preparing a wafer defect map to visually represent the location and type of the wafer defects, and preparing one or more charts or graphs to statistically represent defect characteristics are performed electronically.

19. The method according to claim 18, wherein identifying a location and type of wafer defects, and determining a composition of the wafer defects are also performed electronically.

20. The method according to claim 11, further comprising analyzing the one or more charts or graphs to determine appropriate corrective action in a wafer fabrication process.

METHOD OF IDENTIFYING AND ANALYZING SEMICONDUCTOR CHIP DEFECTS

ABSTRACT OF THE DISCLOSURE

According to a preferred aspect of this invention, locations of defects on a semiconductor wafer are found using semiconductor defect inspection instrumentation. Defect composition can also be determined using inspection instrumentation. Wafer defects are represented on a wafer defect map using markings wherein locations of the markings on the map correspond to the locations of the defects on the wafer. The markings also preferably represent a defect type and/or composition. Color-coded dots, for instance, can be used to represent like defect causes or types with like colors. Graphs can be prepared to display defect characteristics using distributions and skews to facilitate quick statistical analysis of the defects. In this manner, wafer defects can be analyzed quickly and efficiently based on characteristics thereof, including, for example, defect type, composition, and cause. This information can be used to help prevent future defects during mass production, thereby improving yield.

FIG. 1

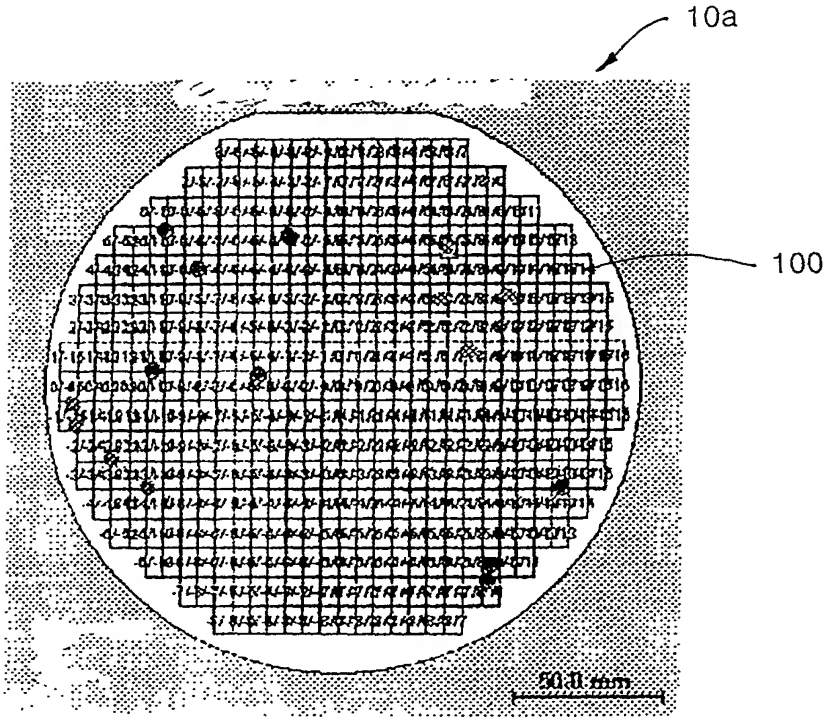

FIG. 2

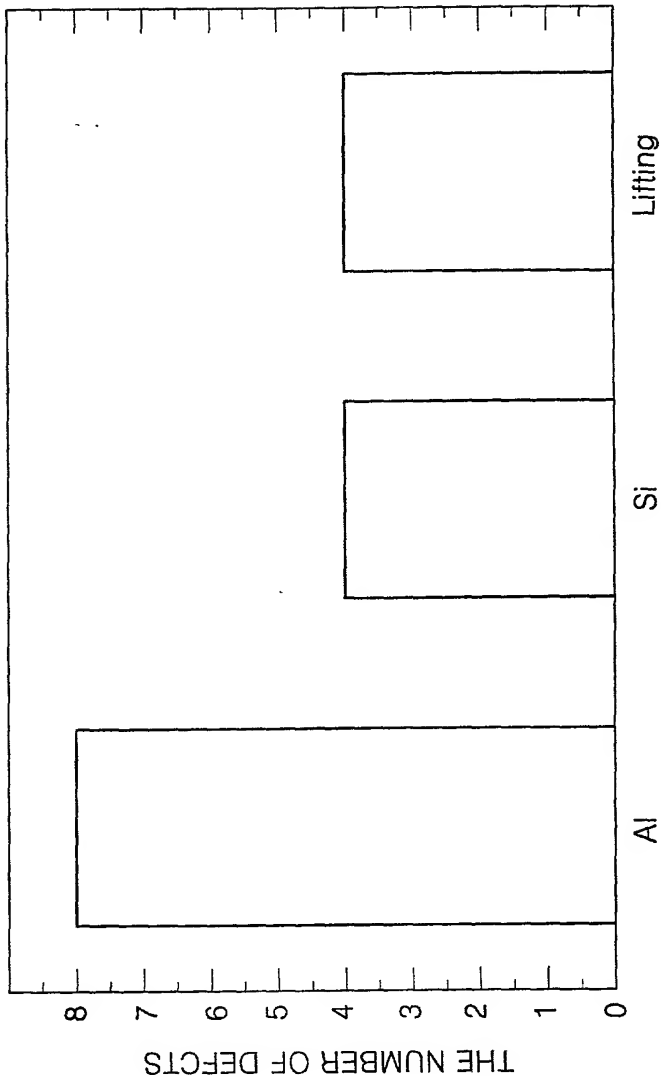

FIG. 3A

FIG. 3B

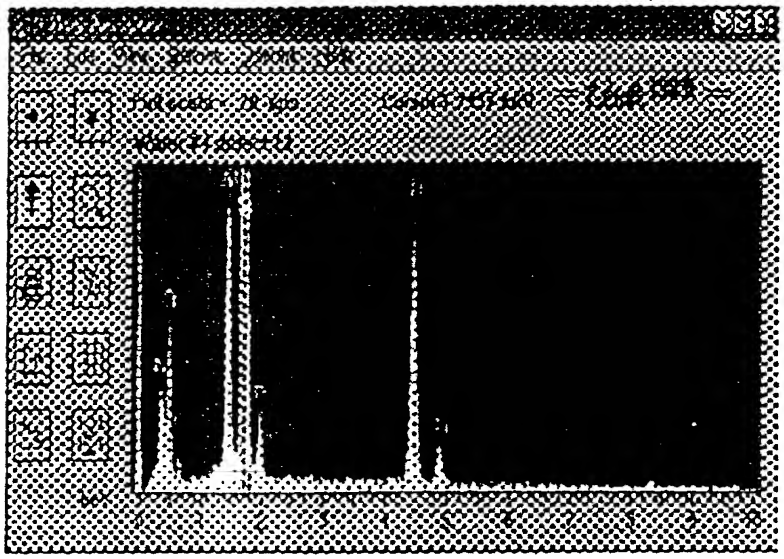

FIG. 3C

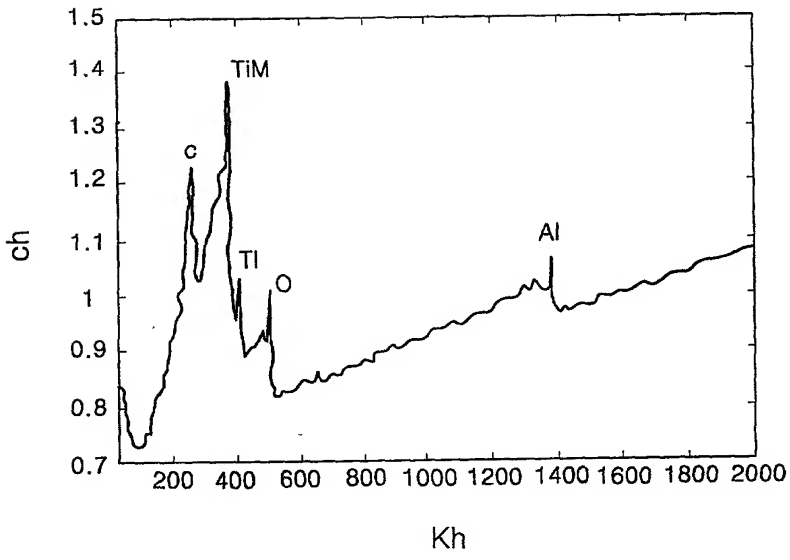
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FIG. 4A
(PRIOR ART)

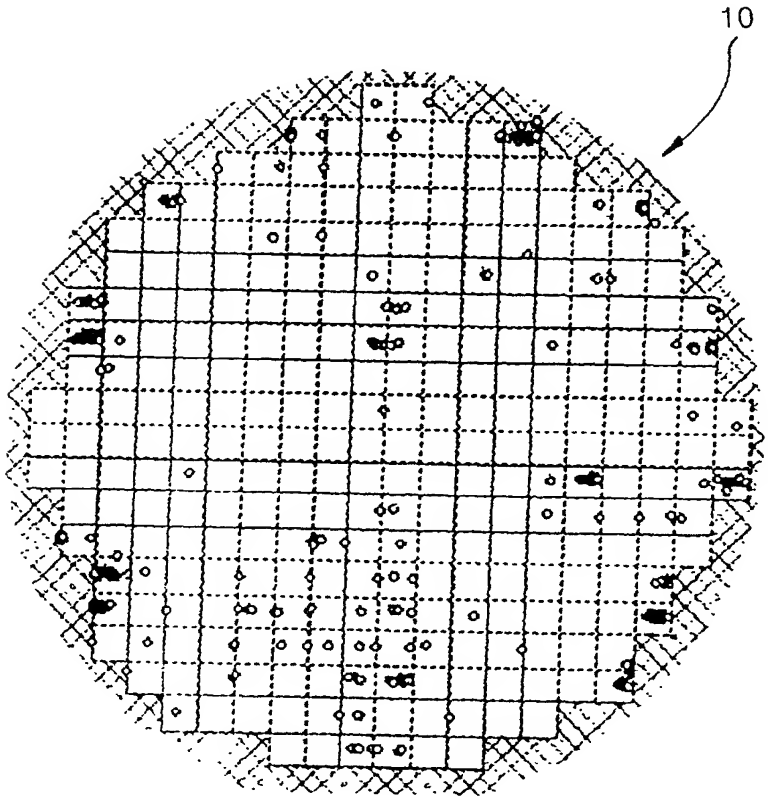
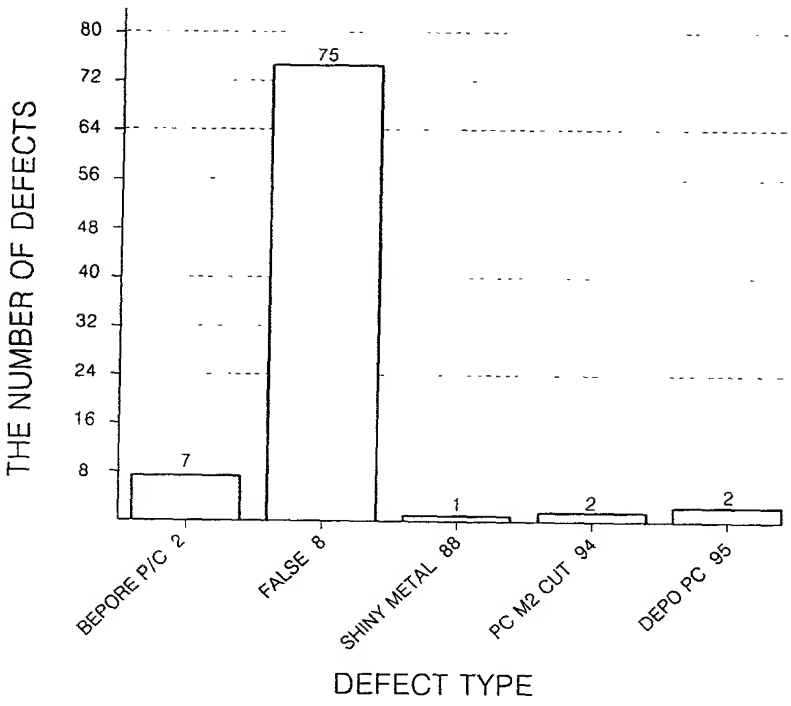


FIG. 4B
(PRIOR ART)



PATENT APPLICATION
Attorney Docket No.8750-017

COMBINED DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled METHOD OF IDENTIFYING AND ANALYZING SEMICONDUCTOR CHIP DEFECTS, the specification of which:

- ☒ is attached hereto.
- ☐ was filed on _____ as Application No. _____
- ☐ and was amended on _____(if applicable)
- ☐ with amendments through _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, Sec. 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Sec. 119 (a)-(d) or §365(b) of any foreign application(s) for patent or inventor's certificate, or §365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Claiming Priority?	
2001-8465	Republic of Korea	20 February 2001	☒	☐
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under Title 35, United States Code, Sec. 119(e) of any United States provisional application listed below:

Provisional Application No.	Filing Date
_____	_____

I hereby claim the benefit under Title 35, United States Code, Sec. 120 or §365(c) of any PCT international application designating the United States of America listed below and,

insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Sec. 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Sec. 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application No.)	(Filing Date)	(Status) (patented, pending, abandoned)

I hereby appoint the following attorneys to prosecute the application, to file a corresponding international application, to prosecute and transact all business in the Patent and Trademark Office connected therewith:

20575
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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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